## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

## 1. REFERENCES

416 Series Order Wire Technical System Description
0416-4606/8875 Wiring Diagram

## 2. DESCRIPTION

2.1. The $-606 / 8875$ system configuration consists of the basic 416 system as described in the 416 Series Order Wire General System description with the addition of a 41687 Multi- Channel Interface module for six channel capability. In the $-606 / 8875$ system configuration, the 41632 DTMF Address Decoder is replaced by the 41662 Multi-Channel DTMF Address Decoder, which provides DTMF detection and decoding for six channels. The six 4-wire ports have balanced inputs and outputs. Channel 6 of the 41687 Multi-Channel Interface is connected through a 41675 Switched Network Interface to a 2-wire subscriber line. The $-606 / 8875$ system configuration also includes a stand alone 41688 8W/4W Bridge.
2.2. The 41687 Multi-Channel Interface module provides switchable connections between the Order Wire RCV/XMT port and six 4-wire ports. Amplifiers on the 41687 module provide impedance matching as well as variable gain for level control. Channel selection is controlled by dedicated push-on/push-off switches located on the front panel. The channel selector switches are equipped with built-in LED's which provide visual indication of the associated channel's status (flashing for incoming call, illuminated for channel selected, and extinguished for channel idle). Since each channel has independent control/status indication, it is possible to select none, all, or any combination of channels at one time.
2.3. The 41675 Switched Network Interface provides ring detection, loop current sink, 4-wire to 2-wire hybrid, and amplifiers for isolation on the rear panel terminal blocks for additional hybrid balance adjustment, if required. The 41675 SNI module status (on hook/off hook) is controlled by the Channel 6 push button switch. When Channel 6 is selected, the 41675 SNI is activated (off hook).
2.4. The 41688 8W/4W Active Bridge has gain available and can be adjusted for 0dB insertion loss or can accommodate various levels from port to port within a 23 dB range.

## 3. SIGNAL FLOW

3.1. TRANSMIT PATH

The output of the 41651 Transmit module (XMT test jacks) is routed to the Order Wire XMT input of the 41687 Multi-Channel Interface. The Order Wire input of the Interface is routed through analog switches to 4 -wire ports, channels 1-5 of the Order Wire, and to the 4 -wire input of the 41675 Switched Network Interface. CH 1 XMT of the 41687 Multi-Channel Interface connects to A1 and A2 on the rear panel. CH 2 XMT connects to B1 and B2 on the rear panel. CH 3 XMT connects to C 1 and C 2 . CH 4 XMT connects to C5 and C6. CH 5 XMT connects to C7 and C8. CH 6 XMT connects to the 4 W receive of the 41675 Switched Network Interface. The 4 W receive routes through a 4-wire to 2 -wire hybrid to the 2 W SNI terminals, G9 and G10, on the rear panel.

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

### 3.2. RECEIVE PATH

Inputs on CH 1 RCV (B1 and B2), CH 2 RCV (D1 and D2), CH 3 RCV (D3 and D4), CH 4 RCV (D5 and D6), CH 5 RCV (D7 and D8), are connected to Channels 1-5, respectively, on the 41687 Multi-Channel Interface. The 2W SNI input (G9 and G10) is connected to the 2-wire port on the 41675 Switched Network Interface. The 4 W transmit on the 41675 is connected to CH 6 RCV on the 41687 Multi-Channel Interface. Channels 1-6 on the 41687 are routed out the Order Wire receive output (pins 9 and 10) of the 41687 and into the receive port on the 41650 Receive module (RCV test jacks).
3.3. AUXILIARY BRIDGE (LEGS 1 THROUGH 8)

The ports of the $8 \mathrm{~W} / 4 \mathrm{~W}$ Bridge in J3 are all wired to the rear panel. An input at any of LEGS 1, 2, 3, 4, 5, 6, 7 , or 8 is routed to all outputs of LEGS $1,2,3,4,5,6,7$, or 8 except its own output.

## 4. ACCESSING THE SWITCHED NETWORK INTERFACE

### 4.1. FROM THE ORDER WIRE

4.1.1. To access the 2 W line from the Order Wire press the CH 6 push button on the front panel. This will activate the 41675 module to the off hook state. When dial tone is returned to the user by the 2-wire equipment, the desired number may be accessed using the DTMF signals generated from the front panel keypad.
4.2. FROM THE 2-WIRE EQUIPMENT
4.2.1. A user may call into the Order Wire from the public network by dialing the number of the 2-wire line connected to the 41675 SNI module. The 41675 module will detect ring voltage and produce audible and visual alerts for CH 6 on the Order Wire.

To answer the call, enable CH 6 on the front panel and pick up the handset.

### 4.3. TERMINATING A CALL

4.3.1. A call on the 2-wire line is terminated by deselecting CH 6 on the front panel.
5. INSTALLATION
5.1. $\quad$ Refer to Table B and wiring diagram 0416-4606/8875 for the required rear panel terminal block connections for system operation. The terminal strips are designed to make a crimp connection on the wire when the screw is tightened. This eliminates the need to install lugs to terminate the wires.
5.2. The Order Wire terminal is shipped with the mounting flanges positioned for a 19-inch rack. If the terminal is to be installed in a 23 -inch rack, remove the flanges and reverse their orientation to accommodate the 23inch rack.

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

## 6. ALIGNMENT

6.1. Alignment of the Order Wire has been performed at the factory. Upon installation the levels should be verified and adjusted as required. Attachment A lists all levels, impedances, etc. for the $-606 / 8875$ system configuration.

Whenever a signal generator is inserted into one of the test points, the port may be double terminated, resulting in an input signal 3.5 dB lower than the dBm reading. To perform an alignment, either bridge the output of the generator with an AC voltmeter when it is inserted into the port and set to the level specified by Attachment A, or remove the equipment (or module) that is providing the termination.

If it is unknown whether a reading of an output level is to be taken as a bridging measurement or with the meter terminated, take a bridging reading and compare it to the terminated reading. If a 3.5 dB difference is noted, the bridging measurement is correct. If a 6 dB difference is noted, the terminated measurement is correct.

### 6.2. VF TRANSMIT LEVEL

6.2.1. Insert a 1 KHz test tone from a signal generator into the TEST TONE jacks at a level of -16 dBm .
6.2.2. Connect an AC voltmeter (bridging) to the XMT jacks. Read the level specified by Attachment A. Adjust R58 (course) or R59 (fine) on the 41651 Transmit, if required.
6.3. DATA TRANSMIT LEVEL
6.3.1. Insert a 1 KHz test tone from a signal generator into the EXT XMT IN jacks. Set the level as specified by Attachment A.
6.3.2. Connect an AC voltmeter (bridging) to the XMT jacks. Read the level specified by Attachment A. Adjust R65 on the 41651 Transmit, if required.
6.4. TRANSMIT SIGNALING LEVEL
6.4.1. Connect an AC voltmeter (bridging) to the XMT jacks.
6.4.2. Go off hook and select one of the digits on the keyboard. Read the level specified by Attachment A. Adjust R8 on the 416-111 Front Motherboard on the front panel, if required.
6.5. VF RECEIVE LEVEL
6.5.1. Insert a 1 KHz test tone from a signal generator into the RCV jacks. Set the level as specified by Attachment A.
6.5.2. Connect an AC voltmeter (terminate with $600 \Omega$ ) to the 4 W OUT jacks. Read a level of +7 dBm . Adjust R40 on the 41650 Receive, if required.
6.6. DATA RECEIVE LEVEL
6.6.1. Insert a 1 KHz test tone from a signal generator into the RCV jacks. Set the level as specified by Attachment

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

## A.

6.6.2. Connect an AC voltmeter (terminate if required) to the EXT RCV OUT jacks. Read the level specified by Attachment A. Adjust R43 on the 41650 Receive, if required.
6.7. SIX CHANNEL INTERFACE LEVELS
6.7.1. Turn power off. Remove the 41687 Multi-Channel Interface module and insert a 42067 Extender Card into the module position. Insert the 41687 module into the Extender Card. Turn power on.
6.7.2. Insert a 1 KHz test tone from a signal generator into the TEST TONE jacks at a level of -16 dBm .
6.7.3. Set the channel select push button switches on the front panel such that only channel 1 is selected. Connect an AC voltmeter (terminate if required) to pins 11 and 12 on the Extender Card. Read the level specified by Attachment A for CH1 XMT. Adjust R75 on the 41687 module, if required.
6.7.4. Set the channel select switches such that only Channel 2 is selected. Move the AC voltmeter (terminate if required) to pins 13 and 14 on the Extender Card. Read the level specified by Attachment A for CH 2 XMT. Adjust R74 on the 41687 module, if required.
6.7.5. Set the channel select switches such that only Channel 3 is selected. Move the AC voltmeter (terminate if required) to pins 15 and 16 on the Extender Card. Read the level specified by Attachment A for CH 3 XMT. Adjust R45 on the 41687 module, if required.
6.7.6. Set the channel select switches such that only Channel 4 is selected. Move the AC voltmeter (terminate if required) to pins 17 and 18 on the Extender Card. Read the level specified by Attachment A for CH 4 XMT. Adjust R44 on the 41687 module, if required.
6.7.7. Set the channel select switches such that only Channel 5 is selected. Move the AC voltmeter (terminate if required) to pins 19 and 20 on the Extender Card. Read the level specified by Attachment A for CH 5 XMT. Adjust R13 on the 41687 module, if required.
6.7.8. Set the channel select switches such that only Channel 6 is selected. Move the AC voltmeter (bridging) to pins 21 and 22 on the Extender Card. Read the level specified by Attachment A for CH 6 XMT. Adjust R12 on the 41687 module, if required.
6.7.9. Move the signal generator to pins Y and Z on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH 6 RCV. Move the AC voltmeter (terminated) to the 4W OUT jacks and read a level of +7 dBm . Adjust R29 on the 41687 module, if required.
6.7.10. Set the channel select switches such that only Channel 5 is selected. Move the signal generator to pins W and $X$ on the Extender Card. Set the level specified by Attachment A for CH 5 RCV. Read a level of +7 dBm on the AC voltmeter. Adjust R30 on the 41687 module, if required.

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

6.7.11. Set the channel select switches such that only Channel 4 is selected. Move the signal generator to pins $U$ and V on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH 4 RCV. Read a level of +7 dBm on the AC voltmeter. Adjust R61 on the 41687 module, if required.
6.7.12. Set the channel select switches such that only Channel 3 is selected. Move the signal generator to pins $S$ and T on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH 3 RCV. Read a level of +7 dBm on the AC voltmeter. Adjust R62 on the 41687 module, if required.
6.7.13. Set the channel select switches such that only Channel 2 is selected. Move the signal generator to pins P and R on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH 2 RCV. Read a level of +7 dBm on the AC voltmeter. Adjust R 91 on the 41687 module, if required.
6.7.14. Set the channel select switches such that only Channel 1 is selected. Move the signal generator to pins $M$ and N on the Extender Card. Set the signal generator to 1 KHz at the level specified by Attachment A for CH 1 RCV. Read a level of +7 dBm on the AC voltmeter. Adjust R92 on the 41687 module, if required.
6.7.15. Turn power off. Disconnect the signal generator and AC voltmeter. Remove the 41687 module and Extender Card. Reinstall the 41687 module in its position.
6.8. SWITCHED NETWORK INTERFACE LEVELS
6.8.1. With power off, remove the 41675 Switched Network Interface module from J4 and install an Extender Card in its place. Insert the 41675 module into the Extender Card and turn power on.

NOTE: Enable the 41675 SNI module by depressing the CH 6 push button. Then call a telephone (with the DTMF keypad on the Order Wire) which can be left off hook while level alignment is performed on the 41675 SNI module. This will eliminate dial tone and allow levels to be adjusted with actual use conditions. The 41675 SNI module can be reset to the idle (on hook) state by selecting the DTMF (\#) digit.
6.8.2. Connect a DC ammeter in series with the 2-wire SNI line (G9 and G10 on the rear panel). Establish a call on the 2-wire line and verify a loop current of 20 to 30 mA .
6.8.3. Connect a signal generator to pins P and R on the Extender Card. Set the signal generator frequency to 1 KHz at the level specified by Attachment A.
6.8.4. Connect a "floating" (earth ground isolated at the AC supply) AC voltmeter (bridging) to pins M and N (2W SNI) on the Extender Card. The signal ground side of the AC voltmeter must be isolated from loop current through a 2 uf capacitor. Read the level specified by Attachment A. Adjust R63 on the 41675 SNI module, if required.
6.8.5. Connect a "floating" signal generator (earth ground isolated at the AC supply) to pins M and N (2W SNI) on the Extender Card. The signal ground side of the signal generator must be isolated from loop current by the 2 uf capacitor. Set the signal generator level as specified by Attachment A.
6.8.6. Connect the AC voltmeter (bridging and not "floating") to pins $U$ and $V$ on the Extender Card. Read the level specified by Attachment A. Adjust R35 on the 41675 SNI module, if required.

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

6.8.7. With the AC voltmeter still connected as in step 6.8.6., connect the signal generator (not floating) to pins $P$ and R on the Extender Card. Set the signal generator level as specified by Attachment A. Adjust R24 and select various capacitance values with S2 on the 41675 SNI module to obtain a minimum reading on the AC voltmeter.

NOTE: It may be necessary to utilize the Line Build Out (LBO, H9 and H10 on the rear panel) if a satisfactory null cannot be obtained (a reading at least 25 dB below the level observed in step 6.8.6.). Adjust R24 and S2 for the lowest possible reading, then add capacitance/resistance to the LBO and readjust R24 and S2 until a satisfactory null is obtained.
6.8.8. Turn power off and remove the 41675 SNI module from the Extender Card. Remove the Extender Card and install the 41675 SNI module in J4.
6.9. $8 \mathrm{~W} / 4 \mathrm{~W}$ AUXILIARY BRIDGE LEVELS (J3)
6.9.1. Turn power off. Remove the 41688 8W/4W Active Bridge in J3. Insert a 42067 Extender Card into the module position. Insert the 41688 8W/4W Active Bridge into the 42067 Extender Card. Turn power on.
6.9.2. Connect a signal generator to pins 21 and 22 (LEG 1 IN), of the 42067 Extender Card. Set the frequency to 1 KHz , at the level specified by Attachment A for LEG 1 IN. Connect the AC voltmeter (terminate if required) to pins F and H (LEG 2 OUT). Read the level specified by Attachment A. Adjust R2 on the 41688 module, if required.
6.9.3. Connect the AC voltmeter (terminate if required) to pins $K$ and $L$ (LEG 3 OUT). Read the level specified by Attachment A. Adjust R3 on the 41688 module, if required.
6.9.4. Connect the AC voltmeter (terminate if required) to pins M and N (LEG 4 OUT). Read the level specified by Attachment A. Adjust R4 on the 41688 module, if required.
6.9.5. Connect the AC voltmeter (terminate if required) to pins R and $S$ (LEG 5 OUT). Read the level specified by Attachment A. Adjust R5 of the 41688 module, if required.
6.9.6. Connect the AC voltmeter (terminate if required) to pins T and U (LEG 6 OUT). Read the level specified by Attachment A. Adjust R6 of the 41688 module, if required.
6.9.7. Connect the AC voltmeter (terminate if required) to pins W and $X$ (LEG 7 OUT). Read the level specified by Attachment A. Adjust R7 of the 41688, if required.
6.9.8. Connect the AC voltmeter (terminate if required) to pins Y and Z (LEG 8 OUT). Read the level specified by Attachment A. Adjust R8 of the 41688, if required.
6.9.9. Connect the signal generator to pins 19 and 20 (LEG 2 IN ). Set the signal generator frequency to 1 KHz . Set the signal generator level as specified by Attachment A.

## 416 SERIES ORDER WIRE

## -606/8875 SYSTEM DESCRIPTION

6.9.10. Leave the AC voltmeter connected (terminate if required) to pins Y and Z (LEG 8 OUT). Read the level specified by Attachment A. Adjust R10 on the 41688 module, if required.
6.9.11. Connect the AC voltmeter (terminate if required) to pins D and E (LEG 1 OUT). Read the level specified by Attachment A. Adjust R1 on the 41688 module, if required.
6.9.12. Connect the signal generator to pins 16 and 17 (LEG 3 IN ). Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as in step 6.9.11. Adjust R11 on the 41688 module, if required.
6.9.13. Connect the signal generator to pins 14 and 15 (LEG 4 IN ). Set the signal generator level as specified by Attachment A. Read the same level as on the AC voltmeter as in step 6.9.11. Adjust R12 on the 41688 module, if required.
6.9.14. Connect the signal generator to pins 11 and 12 (LEG 5 IN ). Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as in step 6.9.11. Adjust R13 on the 41688 module, if required.
6.9.15. Connect the signal generator to pins 9 and 10 (LEG 6 IN). Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as in step 6.9.11. Adjust R14 on the 41688 module, if required.
6.9.16. Connect the signal generator to pins 6 and 7 (LEG 7 IN). Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as in step 6.9.11. Adjust R15 on the 41688 module, if required.
6.9.17. Connect the signal generator to pins 4 and 5 (LEG 8 IN ). Set the signal generator level as specified by Attachment A. Read the same level on the AC voltmeter as in step 6.9.11. Adjust R16 on the 41688 module, if required.
6.9.18. Turn power off. Remove the Extender Card and re-install the 41688 module in J3.



## 41620 REGULATED POWER SUPPLY

## UNIT DESCRIPTION, ISSUE 08 P3

## 1. REFERENCES

1416-1202 Regulated Power Supply Schematic
2. GENERAL

The Raven 41620 Regulated Power Supply provides a regulated -20 Volt DC (@ 1.2A max.) output from an unregulated supply.

The 41620 has two input power options available. The 41620-01 regulates an input voltage ranging from -24 to -56 VDC. The $41620-02$ provides a regulated output from either a 110 VAC or a 220 VAC $(50 / 60 \mathrm{~Hz}$ ) source.

The 41620 provides foldback current limiting at an output current of approximately 1.2 amperes. The 41620 can be modified at the factory to increase the maximum output current if required. Included on the 41620 is an ON/OFF power switch and a fuse in series with the input. The output is factory set at -20 VDC but is adjustable from -18 VDC to -24 VDC.

## 3. SPECIFICATIONS

| Input Voltage |  |
| :---: | :---: |
| Option -01 | -24 VDC TO -56 VDC |
| Option-02 | 110 VAC or 220 VAC ( $50 / 60 \mathrm{~Hz}$ ) |
| Output Voltage | -20 VDC regulated |
|  | -18 VDC to -24 VDC adjustment range |
| Output Current | 1 ampere @ - 20 VDC foldback current limiting occurs @ approximately 1.2A |
| Output Voltage Ripple | $\leq 75 \mathrm{mv}$ (full load) |

## 4. THEORY OF OPERATION

Power input to the 41620 is derived from either a -24 to -56 VDC source in the $41620-01$ version or from a 110 VAC or $220 \mathrm{VAC} 50 / 60 \mathrm{~Hz}$ source in the $41620-02$ version.

### 4.1 41620-01 DC OPTION

The DC input voltage is applied between pins R, S, (optionally pin D or pin N) and Ground (pin B) through CR8, fuse F1, power switch S1 and the "DC" strap. The input voltage is then applied to the emitter of the series pass transistor Q1 via R9.

## 41620 REGULATED POWER SUPPLY

## UNIT DESCRIPTION, ISSUE 08 P3

## 4.2. <br> 41620-02 AC OPTION

The AC input is applied to pins U and W with the external ground connected to pin Y or Z . The input voltage completes the circuit through "AC" strap, fuse F1 and power switch S1 to the primary of transformer T1. T1 steps down the incoming 110 VAC or 220 VAC to a nominal 32 VAC.

The 32 VAC is full wave rectified by the silicon bridge rectifier CR1. Capacitor C1 helps eliminate the ripple component on the unregulated DC. The unregulated DC is applied to the emitter of the series pass transistor Q1 via R9.
4.3.
4.5.

DC REGULATOR
U1 is a 723 Integrated Circuit voltage regulator which provides a regulated output to the base of transistor Q2. Q2 provides the current drive to the base of the series pass transistor Q1.

Resistors R11 and R12 form a voltage divider that is referenced to the -20 V regulated output and driven by the "Voltage Reference Output" of the 723. This combination provides a voltage that is fixed in reference to the -20 V regulated output. This voltage drives the "Inverting Input" of the 723. The voltage for the "Non-inverting Input" of the 723 is determined by the setting of R15 in combination with R13 and R14. R15 is used to adjust the -20 V regulated output, which can be monitored at TP1. Both R15 and TP1 are near the switch at the front of the board for easy access.

## 4. FOLDBACK CIRCUITRY

R9, R1, R2, and Q4 comprise a current sensing circuit and determine when foldback occurs. R5 and R6 provide a reference voltage to the inverting input of comparator U 2 .

A -16 VDC supply is derived from the input voltage via $\mathrm{R} 8, \mathrm{CR} 2$, and C 3 to power comparator U 2 . R3, R4, and CR4 provide a secondary reference voltage to the inverting input of comparator U2. These components insure control over the foldback circuitry even when the regulated output voltage drops to 0 .

When the output current exceeds 1.2 A , transistor Q 4 will turn on, causing the output of comparator U 2 to switch. This turns transistor Q3 on which turns transistor Q2 off and limits current flow through the series pass transistor Q1. Diode CR5 protects the output of the 723 regulator when foldback occurs.

CR7 is a "Power On" LED indicator. This LED will be illuminated when the 41620 is turned ON and the regulated output voltage is present.

## 41632 DTMF ADDRESS DECODER

## UNIT DESCRIPTION, ISSUE 08 P1

## 1. REFERENCES

1416-1320 DTMF Address Decoder Schematic
2. GENERAL
2.1. The Raven 41632 DTMF Address Decoder provides 2 of 7 or 2 of 8 DTMF tone detection for one, two, three, or four digit addressing. For call decoding, digit selection is performed by setting DIP switches (up to four) to respond to the desired digits. A strap selectable interdigit timeout sets the allowable delay time between correct digits. To prevent loading of the receive line, the input to the 41632 module is a balanced high impedance input.
2.2. Two Correct Address outputs are provided. One Correct Address output resets after a strap selectable time period (interdigit/ring-time timeout) or an external reset ("*" or "\#"). The second Correct Address output can only be reset by an external reset, or optionally, the DTMF ALL CLEAR (\#).
2.3. The DTMF ALL CLEAR (\#) and ALL CALL (*) tone pairs have outputs provided. The ALL CALL can be used in two ways. (1) Selecting an ALL CALL tone pair for more than one second allows the ALL CALL output to go active for the duration of the tone. (2) Selecting an ALL CALL tone pair for less than one second allows the ALL CALL $\left(^{*}\right)$ tone to be a generic digit. This allows for group call capabilities (i.e. addresses 121, 122, 123, and 124 would be considered correct addresses when the 41632 module receives the tone sequence $1-2-*$ ).

## 3. SPECIFICATIONS

| Power |  |
| :--- | :--- |
| Environmental | $-20 \mathrm{VDC} @ 50 \mathrm{~mA}$ max. |
| Operating Temperature | $0^{\circ}$ to $50^{\circ} \mathrm{C}$ |
| Storage Temperature <br> Relative Humidity | $-20^{\circ}$ to $+85^{\circ} \mathrm{C}$ |
| Signal Input | 0 to $95 \%$, non-condensing |
| Impedance | $100 \mathrm{~K} \Omega @ 1 \mathrm{KHz}$ |
| DTMF Detect Level | -25 dBm minimum to +6 dBm maximum |
| Minimum Tone Duration | 40 mSec. |
| Signal-to-Noise Ratio | 12 dB minimum |
|  |  |
| Reset Input | Active Ground |
|  |  |
| DTMF Tones | $\pm 1.5 \%$ |
| Detector Bandwidth | $\pm 10 \mathrm{~dB}$ |
| Allowable Twist | 40 mSec. |
| Inter-digit pause detect time | -23 to +7 dBm |
| Signal Level Range |  |

## 41632 DTMF ADDRESS DECODER

## UNIT DESCRIPTION, ISSUE 08 P1

| Timers |  |
| :--- | :--- |
| Inter-Digit Timeout and Ringtime | Minimum $=4.7$ seconds <br> Maximum $=1 \mathrm{~min} .15 \mathrm{sec}$. |
| Timed Correct Address Delay | Minimum $=37 \mathrm{mSec}$. <br> Maximum $=2.4$ seconds |
| Wrong Digit Holdoff | Minimum $=.25$ seconds <br> Maximum $=19$ seconds |
| Outputs <br> ALL CALL, ALL CLEAR, Correct <br> Address 1 \& 2 | Open Collector, ground when active |
| Wrong Digit | Open Collector, -20V when active |
| Logic "1" | Ground |
| Logic "0" | -5VDC |

## 4. <br> ADDRESS DIGIT PROGRAMMING

The 41632 DTMF Address Decoder detects and utilizes Dual Tone Multi-frequency (DTMF) signals to provide selective address decoding functions. DTMF signals are unique tone pairs generated by standard Touch Tone encoder arrays. Each button on a Touch Tone encoder is identified by the pair of frequencies generated when the button is pushed. Four low-group frequencies correspond to the four rows of buttons, and four high-group frequencies correspond to the four columns. The fourth column $(1633 \mathrm{~Hz})$ is typically used only in special control applications.

| 1 | 2 | 3 | A | 697 Hz |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| 4 | 5 | 6 | B | 770 Hz |  |
| 7 | 8 | 9 | C | 852 Hz | LOW GROUP |
| $*$ | 0 | $\#$ | D | 941 Hz |  |
| 1209 Hz | 1336 Hz | 1477 Hz | 1633 Hz |  |  |
|  |  |  |  |  |  |

## 41632 DTMF ADDRESS DECODER

## UNIT DESCRIPTION, ISSUE 08 P1

To program the 41632 DTMF Address Decoder, determine the number of digits to be used (one, two, three, or four) and install the appropriate strap (CA 2) or set the switch SW5 (CA 1):

## Correct Address $1 \quad$ Correct Address 2

One digit Code: SW5 switch $1 \quad$ CA 2 DIGIT 1
Two digit Code: SW5 switch 2 CA 2 DIGIT 2
Three digit Code:
Four digit Code:
SW5 switch $3 \quad$ CA 2 DIGIT 3

SW5 switch $4 \quad$ CA 2 DIGIT 4

Four DIP switches labeled SW1 (1st Digit), SW2 (2nd Digit), SW3 (3rd Digit) and SW4 (4th Digit) are the correct address programming switches. The 4 individual switch positions on each switch correspond to the code from the DTMF tone detector U4. Refer to the table below for digit programming information.
$0=$ off; $1=$ on

| DTMF | Switch Position | DTMF | Switch Position |
| :---: | :---: | :---: | :---: |
| Digit | 1234 | Digit | 1234 |
| 1 | 1000 | 9 | 100 |
| 2 | 01100 | 0 | 010 |
| 3 | 1100 | * | 110 |
| 4 | $\begin{array}{lllll}0 & 0 & 1 & 0\end{array}$ | \# | 001 |
| 5 | 10010 | A | 101 |
| 6 | $\begin{array}{llll}0 & 1 & 1 & 0\end{array}$ | B | $\begin{array}{llll}0 & 1 & 1 & 1\end{array}$ |
| 7 | 1110 | C | $\begin{array}{llll}1 & 1 & 1\end{array}$ |
| 8 | 0001 | D | 0000 |

For example, if the address code of 357 is to be detected, either SW5 switch 3 is selected and/or CA 2 DIGIT 3 is installed. Set the switches on SW1 to correspond to the DTMF digit 3 (1100). Set the switches on SW2 to the DTMF digit 5 (1010). SW3 will be set to correspond to the DTMF digit 7 (1110). SW4 can be set to anything as its setting is ignored in this example.

## 41632 DTMF ADDRESS DECODER

## UNIT DESCRIPTION, ISSUE 08 P1

## 5. THEORY OF OPERATION

5.1. DTMF Tone Detection

The input signal enters the 41632 module on pins D and E and is routed to the input buffer U3A-U3C. Input buffer U3 is high impedance and converts the signal to a single ended format. The signal is then routed to the input of the DTMF detector (U4). U4 detects the DTMF tones. When a valid DTMF tone pair is detected, U4 brings its strobe (pin 15) high, and sets its data lines (Q0, Q1, Q2, and Q3) to the corresponding DTMF tone pair.
5.2. TIMING FUNCTIONS

U2 is a binary ripple counter with an R-C oscillator on its input. The output of U 2 (pin 1) is approximately 27 Hz , and connects to another binary ripple counter (U1). U1 divides the 27 Hz clock in binary steps and provides the resultant frequencies to its Q outputs. The frequencies are used to create the interdigit timeout/ring time, and the enable delay. When the 41632 is in the idle state, U1 is continuously being clocked and stepping through its Q outputs. When a correct digit is detected, U1 is reset to zero to initialize the timing sequence.

The ENABLE DELAY straps are used to enable the Correct Address 1 output (pin F). The INTERDIGIT TIMEOUT/RINGTIME straps provide two functions. The first function is used to set the timeout between valid digits. The second function is used to set the time the Correct Address 1 (pin F) remains active. Only one strap is installed for the interdigit/ringtime. For example, if an interdigit timeout is strapped for 4.7 seconds, then the correct address 1 output (pin F ) will remain active for 4.7 seconds.

### 5.3. ADDRESS DETECTION

DIP switches SW1, SW2, SW3 and SW4 are used to select the digits to be recognized as the correct address. SW1 selects the first digit, SW2 selects the second digit, SW3 selects the third digit, and SW4 selects the fourth digit. The four positions on the switch correspond to the DTMF code. Refer to section 4 of this description for specific information on correct address programming.

Octal counter (U12) provides a sequencing logic high (ground) on one of its eight Q outputs, five of which are used. When U12 is reset, either from an interdigit timeout, wrong digit, or an external reset (pin R), its Q0 output (pin 2) is at logic high. Output Q0 enables U11, a four bit selector via U8A, and selects the data present on its X inputs (SW1). This data is presented at Exclusive NOR gate U9.

When a DTMF digit is detected, U4 brings its strobe active (high), enabling U18, sections A, B, C, and D, and places the DTMF code on its data outputs. These data outputs connect to the Exclusive NOR, U9.

If the data from U7 or U11 (SW data) and U4 (DTMF tone received data) agree, then the DTMF tone is a correct digit. All outputs of U9 are high causing the output of U13A to go high. The output of U13A connects to AND gate U18A, through diode CR2. The output of U18A connects to the CLOCK input of U12. When the correct digit is detected, U18A output goes low. When the tone ends, U18A goes

## 41632 DTMF ADDRESS DECODER

## UNIT DESCRIPTION, ISSUE 08 P1

high, causing U12 to clock to Q1, and U1 to reset. If the CA 2 DIGIT 1 strap is installed, U17B is set, causing transistor Q4 to turn on (pin N, CORRECT ADDRESS LATCHED). Likewise, if the CA 1 SW5 switch 1 is ON, the data input of U17A is set high. As the output of U1 (ENABLE DELAY strap) goes high, the data is latched into U17A, causing Q1 to turn on (pin F, CORRECT ADDRESS 1). For each correct digit detected, U12 is clocked, enabling the different switches (SW5 switch 2, 3, and 4).

If the data from U7 or U11 (SW data) and U4 (DTMF tone received data) disagree, then the DTMF tone is a wrong digit. If any output of U 9 is low, it will cause the output of U13A to stay low. When the wrong digit is detected, U18A output stays high. The output of U18A connects to U18B. The output of U18B goes through time delay R16 and C25, and is inverted by U14C. The output of U14C clocks a high into latch U16A. The output of this latch enables counter U6. During the strap selected wrong digit hold-off period the correct address digit counter U12 and the timed correct address latch (U17A) are held reset. If another DTMF strobe is detected during the hold-off period, the counter will be reset and the hold-off period starts over. When the counter reaches the strap selected time period the latch U16A is reset and the correct address digit counter and the timed correct address latch are enabled. The latch U16A can also be cleared by an "ALL CLEAR" or "RESET" condition which will reset \& disable the counter U6.

The wrong digit function is disabled while Q 1 is on (pin F, CORRECT ADDRESS 1) by the path through CR9 and ST6 to correct address latch (U17A) pin 1. This prevents turning off correct address if another DTMF key is pressed. To defeat this feature remove strap ST6.

The wrong digit hold-off signal is OR'd with the "RESET" signal so that U12 and U17A are also reset by a "RESET" condition.
5.4. The ALL CLEAR (\#) tone pair has an open collector output. When the ALL CLEAR tone is detected, U18D goes low, turning on transistor Q2 (pin K ALL CLEAR). U15A also resets the wrong digit holdoff timer, U6.
5.5. The ALL CALL $\left({ }^{*}\right)$ tone pair has two functions. (1) If the ALL CALL tone pair is present for less than 1 second, then the tone is considered a correct digit if the Group Call option -02 is installed. When the ALL CALL tone is detected, U10A goes high. The output of U10A connects to U18A through diode CR3. The procedure occurs the same as a correct digit as described above. (2) If the ALL CALL tone pair is present for more than 1 second, U19B times out enabling U20C. The output of U20C goes low, turning on transistor Q3 (pin L ALL CALL). When the ALL CALL tone goes off, U20A goes high, resetting U12 and U17B.

## 41632 DTMF ADDRESS DECODER

UNIT DESCRIPTION, ISSUE 08 P1
5.6.
5.7.

## ALL CLEAR RESET OPTION -01

If the ALL CLEAR reset option is installed, the 41632 will reset the interdigit timer (U12), the Correct Address 2 output ( $\operatorname{pin} \mathrm{N}$ ), the Correct Address 1 output (pin F), the wrong digit latch U16A, and the wrong digit hold-off timer U6 upon the receipt of the DTMF digit ALL CLEAR.

GROUP CALL OPTION -02
This allows the caller to contact more than one Order Wire at the same time by using a $\left(^{*}\right)$ as a "wild card". For instance, by dialing $12^{* *}$, all 4 digit phone numbers with 12 as their first two digits would ring.

## 41650 RECEIVE MODULE

## UNIT DESCRIPTION, ISSUE 10

## 1. REFERENCES

1416-1501 Receive Schematic
2.

GENERAL
2.1. The Raven 41650 Receive module provides wideband (data), voice and speaker outputs from a single balanced input. Amplification is provided on all ports, with a 3 -stage low pass filter inserted in the voice and speaker paths. A wide range of input levels can be accepted through the use of level adjustment for all ports. An audible call alert generator is typically included, providing a call indication through the speaker output when enabled. Relay contacts (2 Form C) are available as a simultaneous call indication. The relay is enabled concurrent with audible alert and can be programmed to energize continuously or to cycle on and off with the audible alert.
2.1.1. The -01 option of the 41650 module includes a single frequency signaling detector for use in E\&M signaling systems.
2.1.2. The -02 option of the 41650 module makes the output of SF detector (option -01 above) available for off-board use.
2.1.3. The -03 option adds a single-ended voice output.
2.1.4. The -04A option converts the RCV input to a single-ended $75 \Omega$ port.
2.1.5. The -04B option converts the RCV input to a single-ended high impedance bridging port (typically $10 \mathrm{~K} \Omega$ ).
2.1.6. The -05 option adds capacitors to the feedback loop of both input amplifier stages for high frequency attenuation.

## 41650 RECEIVE MODULE

## UNIT DESCRIPTION, ISSUE 10

## 3. SPECIFICATIONS

| Power | -20VDC @ 200mA max. |
| :---: | :---: |
| Environmental |  |
| Operating Temperature | $0^{\circ}$ to $50^{\circ} \mathrm{C}$ |
| Relative Humidity | $0^{\circ}$ to $95 \%$ non-condensing |
| Input/Output Impedance | $600 \Omega$ balanced, standard |
| Input Level (RCV) | -46 to $+7 \mathrm{dBm} @ 600 \Omega$ |
| VF Frequency Response | $\pm 1 \mathrm{dBm} 0500 \mathrm{~Hz}$ to cutoff frequency, (Ref. @ 1 KHz ) -3 dBm 0 @ $300 \mathrm{~Hz}, \geq 55 \mathrm{~dB}$ down @ $1 / 4$ octave above cutoff frequency. |
| Wideband Frequency | $\begin{aligned} & \pm 1 \mathrm{dBm} 0500 \mathrm{~Hz} \text { to } 30 \mathrm{KHz} \text {, (Ref. @ } 1 \mathrm{KHz} \text { ) }-3 \mathrm{dBm} 0 @ 300 \mathrm{~Hz} \\ & -4 \mathrm{dBm} 0 @ 60 \mathrm{KHz} . \end{aligned}$ |
| Harmonic Distortion | <1\% |
| Signaling Frequency (SF) | Customer specified from 1000 Hz to 3825 Hz |
| Speaker Output | 1 W max into $45 \Omega$ |
| Receive Signaling Relay | Dual Form C rated @ 1A @ 125VAC or (E-Lead) 2A @ 30VDC. |

The 41650 Receive module provides two $600 \Omega$ balanced outputs from one RCV input. One output is for VF , and one is the wideband (data) output. A VF speaker amplifier, an alert tone generator E-Lead relay contacts, and when the -01 option is installed, a signal detector are included on the module.
4.1. INPUT AMPLIFIER

The 41650 Receive module has a single $600 \Omega$ balanced input which is split into two $600 \Omega$ balanced outputs as well as a speaker amplifier output. Transformer T1 provides the balanced input as well as excellent common mode rejection and DC isolation. Input amplifier U6A provides the first stage of gain and its output level is adjusted by potentiometer R36. Amplifier U6B is the second stage of gain and its output level is always set to +6 dBm nom. (optimum input level into the low pass filter) by potentiometer R40. This output drives the wideband amplifier, the VF path, and, when the - 01 Option is installed, the Signaling Detector. Option -05 adds capacitors to the feedback loop of amplifiers U6A and U6B to attenuate their output at frequencies above 16 KHz .

## 41650 RECEIVE MODULE

## UNIT DESCRIPTION, ISSUE 10

### 4.2. WIDEBAND AMPLIFIER

Amplifier U7A is the wideband amplifier and its output level is adjusted by potentiometer R43. This output drives transformer T2 via impedance matching resistor R41. Transformer T2 provides a balanced output as well as DC isolation for the EXT RCV OUT port.
4.3. VF AMPLIFIER
4.3.1. The signal at the output of amplifier U6B is routed through the low pass filter. The low pass filter used on the 41650 Receive module is a 3 D-element active filter which provides a response of $+1,-3 \mathrm{~dB}$ over a frequency range of 300 Hz to the cutoff frequency ( Fc , customer specified), and attenuation of 355 dB of signals one quarter octave above Fc. The low pass filter consists of Operational Amplifiers U1, U2, U3 and associated circuitry.
4.3.2. The output of the low pass filter is routed to the input of amplifier U8A. The path from the low pass filter to U8A is strappable such that with ST-9 removed and ST-E1 \& ST-F1 installed, the signal can be routed through other modules via pin $\mathrm{F}, \&$ return via pin E into U8A. U8A is a fixed gain amplifier \& drives the 4W OUT via impedance matching resistor R58 \& transformer T3, as well as the speaker amplifier.
4.3.3. Option -03 provides a single-ended input (if ST-11 is installed), or single-ended output (if ST-10 is installed) on pin K via resistors R59 and R74 from amplifier U8A. The values of R59 and R74 are factory selected according to the application.

### 4.4. SPEAKER AMPLIFIER

The speaker amplifier consists of U8B, Q5, Q2, Q3, Q4 and associated circuitry. Inputs from the VF path, the sidetone input (from the 41651 Transmit module), and the alert tone generator are summed into the speaker amplifier. An off-board potentiometer (typically a 1 KW 1 W potentiometer on the front panel of the Order Wire) connected to pins U and V acts as a shunt to provide a volume control for the VF and sidetone signals. The volume of the alert tone is not affected by the volume control. The speaker amplifier has a maximum output of 1 W into a $45 \Omega$ speaker with $<2 \%$ harmonic distortion.
4.5. ALERT TONE GENERATOR
4.5.1. The Alert Tone Generator is an option that is more commonly installed than not. It is deleted in cases where another source for the alert tone is more desirable.
4.5.2. Two alert tone frequencies are available \& are selected via 3 programming jumpers. When the jumpers are in the "LO" position, the frequency is 360 Hz . When the jumpers are in the "HI" position, the frequency is 1940 Hz . Potentiometer R72 can be used to adjust the alert tone volume(1 watt max. to .1 watt min.).

## 41650 RECEIVE MODULE

## UNIT DESCRIPTION, ISSUE 10

4.5.3. The Alert Tone Generator consists of U11, U9, and associated components. U11 is a free running oscillator which generates the alert tone $(360 \mathrm{~Hz}$ or 1940 Hz$)$ as well as the output to gate the tone ON and OFF at preset rates through U9. The outputs of U9 are coupled to the speaker amplifier. The ALERT tone is activated by grounding pin R. The ALL CALL tone is activated by grounding pin S (ST-4 installed). The ALL CALL tone is gated at approximately .5 secs. OFF and .5 secs. ON, while the ALERT tone is gated at approximately 1.5 secs. OFF and 1.5 secs. ON.
4.5.4. Activating either the ALERT or ALL CALL energizes relay K1. This two form C relay provides an E-Lead indication as well as driving the ALERT indicator on the Order Wire front panel (when provided). Two modes of operation can be selected, 1) the relay is continuously energized for the duration of the alert tone (CO position of the programming jumper), or 2 ) the relay will cycle on and off at the same rate as the alert tone (CY position of the programming jumper).

### 4.6. SIGNALING DETECTOR

When the -01 option is installed, a signaling detector is included as a part of the 41650 module. The signaling detector consists of a narrow band pass filter (U5A, U4A, U4B, and associated circuitry), a peak detector (D1, R29, R30, C14, C15), and a comparator (U5B). Potentiometer R25 adjusts the overall gain and potentiometer R24 adjusts the center frequency of the filter. When the voltage across C15 exceeds the comparator reference voltage (pin 6 of U5B), the comparator output switches high activating the alert tone generator $(\mathrm{U} 11, \mathrm{U} 9)$ and the receive relay K1 via transistor Q1.
4.7. Option -02 pins out the signal detector output (pin 7 of comparator U5B) on pin W. If strap ST-5 is installed, the output is routed directly from comparator U5B and is active high (GND). If ST-5 is deleted and transistor Q6 and its associated resistors are installed, Q6 inverts the output of U5B, making the output at pin W active low (-20VDC).
4.8. Option -03 provides a single-ended voice input or single-ended voice output when R59, R74, and C36 are installed. The value of each component is determined by the application. A typical use for the input is to sum an auxiliary tone or voice path into the speaker amp. A typical use for the output is to drive the earpiece from a remotely located headset or telephone.
4.9. Option -04 changes the configuration of the input amplifier for a single-ended $75 \Omega$ input (terminating or bridging). Transformer T1 is deleted and a $.33 \mu \mathrm{f}$ ceramic capacitor is installed in its place for DC isolation. Pin C of the 41650 module is the signal input, and pin D is ground. For a $75 \Omega$ terminating input, a $75 \Omega$ resistor is installed across pins C and D . For a high impedance bridging input, the $75 \Omega$ resistor is deleted.
4.10. Option -06 adds capacitance to the feedback loop of both stages of the input amplifier, U6A and U6B. The capacitance value is selected to attenuate frequencies above the spectrum utilized by the wideband (data) port.

## 41651 TRANSMIT MODULE

## UNIT DESCRIPTION, ISSUE 10

## 1. REFERENCES

1416-1511 Transmit Schematic
2.
2.1. The Raven 41651 Transmit Module provides a single balanced output from multiple VF inputs, a wideband (data) input, and a signaling oscillator. Amplification is provided on all ports, with a 3 -stage low pass filter inserted in the voice path. All ports have potentiometer level adjustment and can accommodate a wide range of output levels.
2.1.1. The -01 Option of the 41651 Module includes a single frequency signaling oscillator for use in $\mathrm{E} \& \mathrm{M}$ signaling systems.
2.1.2 The -02 Option of the 41651 Module includes a ringback tone oscillator for call acknowledgment (typically used only in DTMF selective signaling systems).
2.1.3. The -03A Option converts the XMT output to a single-ended $75 \Omega$ port.
2.1.4. The -03B Option converts the XMT output to a single-ended high impedance bridging port.
2.1.5. The -04 Option supplies talk battery for a remote MIC at pins M and N (4-wire input).
2.1.6. The -05 Option XMT relay will prevent any transmission at pins K and L until the transmit path is enabled at pin Y (typically DTMF correct address) or at pin Z (typically off hook condition).

## 41651 TRANSMIT MODULE

## UNIT DESCRIPTION, ISSUE 10

## 3. SPECIFICATIONS

| Power | -20VDC @ 50mA max |
| :---: | :---: |
| Environmental |  |
| Operating Temperature | $0^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$ |
| Relative Humidity | $0 \%$ to $95 \%$ non-condensing |
| Input/Output Impedance | $600 \Omega$ balanced, standard |
| Output Level (XMT) | +7 dBm max. -46dBm min. @ 600 |
| Idle Noise (XMT) | $<10 \mathrm{dBrnC0}$ |
| VF Frequency Response (Ref. @ 1KHz) | $\pm 1 \mathrm{dBm} 0500 \mathrm{~Hz}$ to cutoff frequency |
|  | -3 dBm 0 @ 300 Hz |
|  | $\geq 55 \mathrm{~dB}$ down @ 1/4 octave above cutoff frequency |
| Wideband Frequency Response (Ref. @ 1KHz) | $\pm 1 \mathrm{dBm} 0500 \mathrm{~Hz}$ to 30 KHz |
|  | $-3 \mathrm{dBm} 0 @ 300 \mathrm{~Hz},-4 \mathrm{dBm} @ 60 \mathrm{KHz}$ |
| Harmonic Distortion | <1\% |
| Signaling Frequency (SF) | Customer specified from 1000 Hz to 3825 Hz |

## 4. THEORY OF OPERATION

The 41651 Transmit Module has five $600 \Omega$ balanced inputs which are summed into one output. Four of these inputs are for VF and one is the wideband (data) input. In addition, the -01 Option signaling oscillator, and the -02 Option ringback oscillator are summed into the wideband path. Output amplifier U7B combines the VF and wideband paths and drives the output transformer T 1 via impedance matching resistor R61.

### 4.1. VF AMPLIFIER

4.1.1. $\quad \mathrm{VF}$ signals enter the module at the DTMF input (pins W and X ), the 4 -wire input (pins M and N ), the TEST TONE input (pins $U$ and $V$ ), and the MIC input (pins $S$ and $T$ ) which also provides talk battery to the microphone. These inputs are all balanced with $600 \Omega$ impedance. Unused inputs need no external termination.

## 41651 TRANSMIT MODULE

## UNIT DESCRIPTION, ISSUE 10

4.1.2 All VF signals are summed at pins 2 and 6 of the differential summing amplifier, U6. The signal at the output of U6B (pin 7) is coupled to the low pass filter and also to pin $P$ which provides local sidetone. The path from U6B to the low pass filter is strappable such that with the strap removed, the signal can be routed through other modules via pin P , and return via pin R into the low pass filter.
4.1.3. The low pass filter used in the 41651 Transmit is a 3 D-element active filter which provides a response of $+1,-3 \mathrm{~dB}$ over a frequency range of 300 Hz to the cutoff frequency ( Fc , customer specified), and attenuation of $\geq 55 \mathrm{~dB}$ of signals one quarter octave or more above Fc . The low pass filter consists of operational amplifiers U1, U2, U3 and associated circuitry. The output of the low pass filter is routed to the input of amplifier U7B via potentiometer R58.

### 4.2. WIDEBAND AMPLIFIER

Wideband signals enter the 41651 Transmit Module on pins F and H and are routed to transformer T2 which provides a balanced input as well as excellent common mode rejection and DC isolation. U7A is the wideband amplifier and potentiometer R65 adjusts the level of the wideband path.
4.3. OUTPUT AMPLIFIER

Amplifier U7B is a single stage amplifier which provides a maximum output of +7 dBm into a $600 \Omega$ load at pins K and L . The gain of U7B is fixed at one of two levels, selected by a programming jumper. The "LG" jumper (ST6) sets the gain at 0 dB and should be used when the output level of the 41651 Module is -10 dBm (@ 600 $\Omega$ ) or less. The normal gain of U7B is +15 dB which is used when the output level of the 41651 Module is greater than -10 dBm (@ 600 ), or when Option -03A or Option -03B is installed.

### 4.4. SIGNALING OSCILLATOR

When the -01 Option is installed, a signaling oscillator is included as a part of the 41651 Module. The signaling oscillator consists of U4, U5 and associated circuitry. The oscillator can be enabled by applying the appropriate voltage to pin D (if ST1 is installed) or pin J. If -01A is installed, -20VDC applied to pins D or J will enable the oscillator, or if -01B is installed, ground on pins D or J will enable the oscillator. The frequency of the signal oscillator is adjusted by R24. The output of the oscillator is coupled through C15 to R35. The oscillator signal then goes to pin 6 of output amplifier U7B and is summed into the transmit output.

## 41651 TRANSMIT MODULE

## UNIT DESCRIPTION, ISSUE 10

4.5.
4.8.
4.7.

## RINGBACK OSCILLATOR

The -02 Option provides ringback tones for call acknowledgment. Oscillator/counter U8 digitally generates the required frequencies when enabled by a ground at pin Y. U9 gates the frequencies to create a ringback tone. The signal then goes to U7B and thus to the transmit output.

## 4.6. <br> .6. SINGLE ENDED OUTPUT

The - 03 Option converts the output amplifier for a single-ended $75 \Omega$ output (terminating or bridging). Transformer T1 and resistor R61 are deleted and a $.33 \mu \mathrm{f}$ ceramic capacitor and a $3.3 \mathrm{~K} \Omega$ resistor are installed. For Option -03A, a $75 \Omega 1 \%$ resistor is included to terminate the port. For Option -03B, the $75 \Omega$ resistor is deleted for high impedance (typically $3.3 \mathrm{~K} \Omega$ ) bridging port.

## TALK BATTERY

The - 04 Option provides talk battery for the use of a remote handset or headset microphone.

## TRANSMIT RELAY

The -05 Option, relay K1, isolates the circuitry on the 41651 Module from the transmit port to minimize idle noise. The relay is energized and connects the transmit path when an off hook condition exists, or when ringback is being transmitted.

## UNIT DESCRIPTION, ISSUE 03 P1

## 1. REFERENCES

1416-1850 4-Way or 6-Way/4-Wire Active Bridge Schematic
2. GENERAL
2.1. The Raven 41685 4-Way or 6-Way/4-Wire Active Bridge provides a multipath interface between 4 ports (or 6 ports with Option -01 installed) on a 4 -wire basis. An input at one of the ports is routed through to the output of all other ports, with a minimum of interchannel crosstalk. All inputs and outputs are transformer coupled and are balanced. Potentiometer adjustments on all inputs and outputs allow input level coordination and through path gain adjustments.

## 3. SPECIFICATIONS

Power Input
Environmental
Operating Temperature $\quad 0^{\circ}$ to $50^{\circ} \mathrm{C}$
Storage Temperature
Relative Humidity
Inputs
Input Impedance $600 \Omega$ balanced
Input Level
-40 to +7 dBm
Outputs
Output Impedance
$600 \Omega$ balanced
Output Level
Through Path Adjustment, Max
Interchannel Crosstalk <-50dB @ 1 KHz and unity gain
4. THEORY OF OPERATION

### 4.1. INPUT CIRCUITRY

4.1.1. Each of the four inputs (six if Option -01 is installed) consists of an input transformer, impedance matching resistor, and an amplifier.
4.1.2. For INPUT LEG 1, R19 is used for impedance matching of the input transformer T7. The input amplifier for INPUT LEG 1 consists of U-2A, R31, R25, and potentiometer R7.

## UNIT DESCRIPTION, ISSUE 03 P1

4.1.3. Signals present at INPUT LEG 1 (pins 21 and 22) are coupled through input transformer T7. The signal is then passed through R31, to the input of amplifier U-2A. R25 and potentiometer R7 provide a gain adjustment of -14 to +19 dB for amplifier $\mathrm{U}-2 \mathrm{~A}$, and presents the signal at pin 1 of $\mathrm{U}-2 \mathrm{~A}$.
4.1.4. All other inputs have circuitry identical to INPUT LEG 1 and operate the same.
4.1.5. For INPUT LEG 2, R20 is used for impedance matching of the input transformer T8. The input amplifier for INPUT LEG 2 consists of U-2B, R26, R32, and potentiometer R8.
4.1.6. For INPUT LEG 3, R21 is used for impedance matching of the input transformer T9. The input amplifier for INPUT LEG 3 consists of U-4A, R33, R27, and potentiometer R9.
4.1.7. For INPUT LEG 4, R22 is used for impedance matching of the input transformer T10. The input amplifier for INPUT LEG 4 consists of U-4B, R28, R34, and potentiometer R10.
4.1.8. For INPUT LEG 5 (if Option -01 is installed), R23 is used for impedance matching of the input transformer T11. The input amplifier for INPUT LEG 5 consists of U-6A, R35, R29, and potentiometer R11.
4.1.9. For INPUT LEG 6 (if Option -01 is installed), R24 is used for impedance matching of the input transformer T12. The input amplifier for INPUT LEG 6 consists of U-6B, R30, R36, and potentiometer R12.
4.2. OUTPUT AMPLIFIERS
4.2.1. Each LEG output is driven by a 3-input (or 5 -input if Option -01 is installed) summing amplifier. The output of the summing amplifier is transformer coupled to provide a balanced output.
4.2.2. The output amplifier for OUTPUT LEG 1 consists of R43, R49, potentiometer R1, U-1A, and transformer T1. R43 provides impedance matching. Resistor Network RN1 sums the inputs from LEGs 2, 3, 4, 5, and 6, (LEGs 5 and 6 are installed for Option -01 only).
4.2.3 Signals present at the summing network (RN1) of OUTPUT LEG 1 are summed and presented to the output amplifier, U-1A. Potentiometer R1 and resistor R49 provide a gain adjustment of -13 to +19 dB . The signal is presented at pin 1 of $\mathrm{U}-1 \mathrm{~A}$ and routed to output transformer T1. The signal is coupled through to OUTPUT LEG 1 (pins D and E).
4.2.4 All other outputs have identical circuitry as OUTPUT LEG 1, and operate the same.
4.2.5. The output amplifier for OUTPUT LEG 2 consists of R44, R50, potentiometer R2, U-1B, and transformer T2. R44 provides impedance matching. Resistor Network RN2 sums the inputs from LEGs $1,3,4,5$, and 6 .

## UNIT DESCRIPTION, ISSUE 03 P1

4.2.6. The output amplifier for OUTPUT LEG 3 consists of R45, R51, potentiometer R3, U-3A, and transformer T3. R45 provides impedance matching. Resistor Network RN3 sums the inputs from LEGs $1,2,4,5$, and 6 .
4.2.7. The output amplifier for OUTPUT LEG 4 consists of R46, R52, potentiometer R4, U-3B, and transformer T4. R46 provides impedance matching. Resistor Network RN4 sums the inputs from LEGs $1,2,3,5$, and 6.
4.2.8. The output amplifier for OUTPUT LEG 5 (when Option -01 is installed) consists of R47, R53, potentiometer R5, U-5A, and transformer T5. R47 provides impedance matching. Resistor Network RN5 sums the inputs from LEGs $1,2,3,4$, and 6.
4.2.9. The output amplifier for OUTPUT LEG 6 (when Option -01 is installed) consists of R48, R54, potentiometer R6, U-5B, and transformer T6. R48 provides impedance matching. Resistor Network RN6 sums the inputs from LEGs $1,2,3,4$, and 5.
4.3. VOLTAGE REGULATION
4.3.1. U7-B provides regulation for the -10VDC bias voltage. U7-A, CR1, CR2, R57, R58, Q1, Q2, R55, and R56 provide a -10VDC signal ground for the output transformers.

UNIT DESCRIPTION, ISSUE 01 P1

## 1. REFERENCES

1422-1860 RS-232 Bridge Schematic
1422-8860 RS-232 Bridge Block Diagram
2. GENERAL
2.1. The Raven 42286 4-Way or 6-Way RS-232 Active Bridge provides a multipath interface between 4 ports (or 6 ports with Option -01 installed) on a three-signal basis. An input at one of the ports is routed through to the output of all other ports. All input signals and output signals conform to RS232 specifications. There are no adjustments required on this module. This module is designed to operate in a system where only one RS-232 circuit (or LEG) is active at any one time.

## 3. SPECIFICATIONS

Power Input
Startup Current
Environmental
Operating Temperature
Storage Temperature
Relative Humidity
Inputs
Input Impedance
Input Level
Logic
Outputs
Output Impedance
Output Level
Logic
Data Rate
-18 to -75 VDC @ 200 mA max
1.5 Amps max

$$
\begin{aligned}
& \quad 0^{\circ} \text { to }+50^{\circ} \mathrm{C} \\
& -40^{\circ} \text { to }+85^{\circ} \mathrm{C} \\
& 0 \text { to } 95 \% \text { non-condensing }
\end{aligned}
$$

$3 K \Omega$ min
Conforms to RS-232 spec, -12 V to +12 V or Logic levels, 0 to +5 V
Unused inputs are low
$700 \Omega$ minimum
-9 V to +9 V minimum with $3 \mathrm{~K} \Omega$ load
Non-inverting
50 to 112,000 Baud

## 4. THEORY OF OPERATION

### 4.1. INPUT CIRCUITS

4.1.1. Each input circuit (three inputs for each LEG) consists of an RS-232 compliant inverting input buffer and an RC filter designed to eliminate damage from ESD hits. Each LEG input consists of the signals from TXD, DTR, and RTS.
4.1.2. The TXD input of LEG 1 is described here. The signal present at pin 5 passes through an RC filter composed of R1 and C3. From this filter the signal is connected to the input pin of the RS-232 input buffer, U7-A.
4.1.3. All other inputs have circuits identical to LEG 1 TXD and operate the same.
4.1.4. Input signals on LEG 1 inputs appear on the corresponding LEGs $2-6$ outputs. Each output LEG consists of the input signals from any LEG except its own.

### 4.2. OUTPUT CIRCUITS

4.2.1. Each output circuit (three outputs for each LEG) consists of an RS- 232 compliant inverting output buffer and an RC filter designed to eliminate damage from ESD hits. Each LEG output consists of the signals to RXD, DSR, and CTS.
4.2.2. Each buffer of each LEG output is a two input AND gate. One of those inputs is connected to the output of a 4 -input AND gate resulting in a 5 -input AND gate.
4.2.3. The output circuits for the LEG 1 RXD signal consists of AND gate U13-A, output buffer U1-B, and RC filter R2 and C4. The output signal appears on pin E of the edge connector.
4.2.4. All other outputs have identical circuits as OUTPUT LEG 1 RXD, and operate the same.

### 4.3. POWER SUPPLY

4.3.1. The 42286 Module is designed to operate with DC input voltages. The input voltage is converted to -12 VDC and +12 VDC by a switching power supply circuit, PS1.
4.3.2. Logic circuit voltage is obtained from the +12 VDC supply using a linear 5 VDC regulator, VR1.
4.3.3. If AC Input Voltage is required an external AC to DC power supply must be used.

